REMARKS

At the outset, Applicants thank the Examiner for examining the pending application. The Office Action dated March 16, 2009 has been received and its contents carefully reviewed.

Summary of the Office Action

Claims 5, 18, 20, 22, 27 and 32 are rejected.

The Office Actions rejects claims 5, 18, 20, 22, 27 and 32 under 35 U.S.C. 103(a) as being unpatentable over the Applicants' Admitted Prior Art (AAPA) and Tsutsui (US 7,196,701).

Summary of the Response to the Office Action

Applicants have amended claims 5, 18, 22, 27 and 32 to further define the invention. No new matter has been added. Reexamination and reconsideration of the pending claims are respectfully requested.

Rejection Under 35 U.S.C 102(e)

Claim 5 is allowable over the cited references in that claim 5 recites a combination of elements including, for example, "taking a power source voltage having a constant level of less than 2.9V from a power source of a system; supplying the power source voltage having the constant level of less than 2.9V to an interface circuit, a timing controller, a data driving circuit and a gate driving circuit for processing digital signal; and raising or reducing the power source voltage having the constant level of less than 2.9V using a DC-DC converter...".

Claim 18 is allowable over the cited references in that claim 18 recites a combination of elements including, for example, "a power source of a system for generating a power source voltage having a constant level under 2.9V; a DC-DC converter for raising or reducing the power

source voltage having the constant level under 2.9V..., wherein the power source voltage having the constant level under 2.9V is supplied to the interface circuit, the timing controller, the data driving circuit and the gate driving circuit".

Claim 22 is allowable over the cited references in that claim 22 recites a combination of elements including, for example, "generating a second power source voltage having a constant level of less than 2.9V from the first power source voltage of 3.3V using a reducing circuit ; supplying the second power source voltage having the constant level of less than 2.9V to the interface circuit, the timing controller, the data driving circuit, and the gate driving circuit for processing digital signal of the interface circuit, the timing controller, the data driving circuit, and the gate driving circuit".

Claim 27 is allowable over the cited references in that claim 27 recites a combination of elements including, for example, "providing a power source voltage from a power source of a system wherein the power source voltage has a constant level of less than 2.9V; supplying the power source voltage having the constant level of less than 2.9V to the interface circuit, the timing controller, the data driving circuit and the gate driving circuit; generating a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL from the power source voltage having the constant level of less than 2.9V using a DC-DC converter".

Claim 32 is allowable over the cited references in that claim 32 recites a combination of elements including, for example, "generating a second power source voltage having a constant level of less than 2.9V from the first power source voltage of 3.3V using a reducing circuit;

supplying the second power source voltage having the constant level of less than 2.9V to the interface circuit and the timing controller for processing digital signal of the interface circuit and the timing controller".

In Response to Arguments of Office Action, Applicants note that Tsutsui clearly teaches that during the power saving mode, the voltage stays constant at 3.0V, it is considered consistent with the claims because the power supply will not *always* be providing a constant voltage, for example when it is turned off, or for example if there are unforeseen electro-magnetic variations.

To obtain a function peculiar to a specific device, a direct current (DC) voltage used in the specific device must always be constant. In other words, Vdd2 of Tsutsui must always and constantly maintain 3.0V to obtain a function of a power saving mode. If it dose not maintain 3.0V, Tsutsui can't obtain the function of the power saving mode. In addition, VDD2 of Tsutsui is 3.0V, whereas a power source voltage of the claimed invention is 2.9V. Thus, it is a difference of 0.1V between Tsutsui and the claimed invention. A lot of DC voltage levels can be positioned and generated between Tsutsui and the claimed invention. For Instance, 999 numbers of DC voltage levels can be positioned and generated between Tsutsui and the claimed invention. In other words, the DC voltage levels include 2.901V, 2.902V, ..., 2.998V, and 2.999V. Thus, since a lot of DC voltage levels are positioned and generated between Tsutsui and the claimed invention, Tsutsui cannot a power source voltage of 2.9V of the claimed invention across the lots of DC voltages levels. Furthermore, VDD2 of Tsutsui fails to disclose a variation of VDD2 of Tsutsui.

As a result, as VDD2 of Tsutsui has a constant DC voltage unvaried, Tsutsui fails to disclose a power source voltage of the claimed invention.

In clams 5, 18, 22 and 27, a power source voltage having a constant level of less than 2.9V is supplied to an interface circuit, a timing controller, a gate driving circuit and a data driving circuit. On the contrary, VDD2 of Tsutsui is supplied to a D/A converter 12 and an amplifier 14. In other words, VDD2 of Tsutsui is not supplied to a timing controller 18 and a gate driving circuit.

In addition, in claim 32, a power source voltage having a constant level of less than 2.9V is supplied to an interface circuit and a timing controller. On the contrary, VDD2 of Tsutsui is supplied to the D/A converter 12 and the amplifier 14. In other words, VDD2 of Tsutsui is not supplied to the timing controller 18. Instead, VDD1 is supplied to the timing controller 18.

Furthermore, in claims 5, 18 and 27, a power source voltage having a constant level of less than 2.9V is supplied to a DC-DC converter. On the contrary, VDD2 of Tsutsui is not suppied to any DC-DC converter. In AAPA, voltage (VCC) of 3.3V is supplied to a DC-DC converter 6.

None of the cited reference, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicants respectfully submit that claims 5, 18, 22, 27 and 32 and claim 20, which depend therefrom, are allowable over the cited references.

Conclusion

In view of the foregoing, Applicants respectfully request reconsideration and the timely allowance of the pending claims. Should the Examiner feel that there are any issues outstanding after consideration of the Amendment, the Examiner is invited to contact the Applicants' undersigned representative to expedite prosecution.

EXCEPT for issue fees payable under 37 C.F.R. 1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due 37 C.F.R. 1.16 and 1.17 which may be required, including any required extension of time fees, or credit any overpayment to Deposit Account No 50-0310. This paragraph is intended to be **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. 1.136(a)(3).

Respectfully submitted,

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